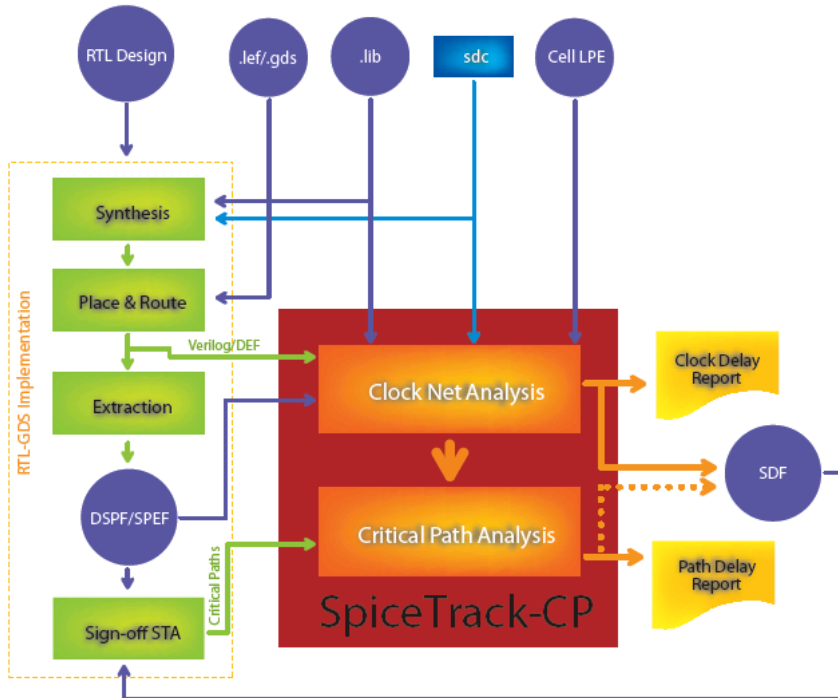


SpiceTrack-CLK

Full-Chip Clock & Critical Path Analysis

SpiceTrack-CLK, based on the powerful and versatile SpiceTrack framework, enables 100% accurate SPICE analysis on full-chip post layout clocks networks and critical paths. using the super-high capacity mSPICE engine, SpiceTrack-CLK can analyze clock networks with millions of elements in a matter of hours.



Features

ROBUST AND OPEN DATABASE

- Reads standard esign file formats such as: LIB, LEF, DEF, SPEF, GDS, Verilog, SDC, and SPICE
- Open database allows easy debugging and flexibility

MULTI-CORNER ANALYSIS Enables simultaneous clock simulations at combinations of parasitic and process corners on different processors

CRITICAL PATH SIMULATION Automatically reads critical path reports from industry standard STA tools and generates reports from SPICE simulations

INSERTION DELAYS AND SKEW Generates insertion delay report in a user-friendly format

SEAMLESS P&R INTEGRATION

- Supports hierarchical verilog & SPEF
- The clock analysis can be integrated into a physical design flow using the TCL interface

SDF BACK-ANNOTATION Generates SDF delays for the clock network for easy back-annotation to STA tools

CAPACITY Using patented mSPICE engine allows unlimited capacity and a practical runtime for all simulations

EASY TO USE

- Intuitive GUI and TCL interface
- Push-button flows for extracting and simulating clock networks from full-chip

