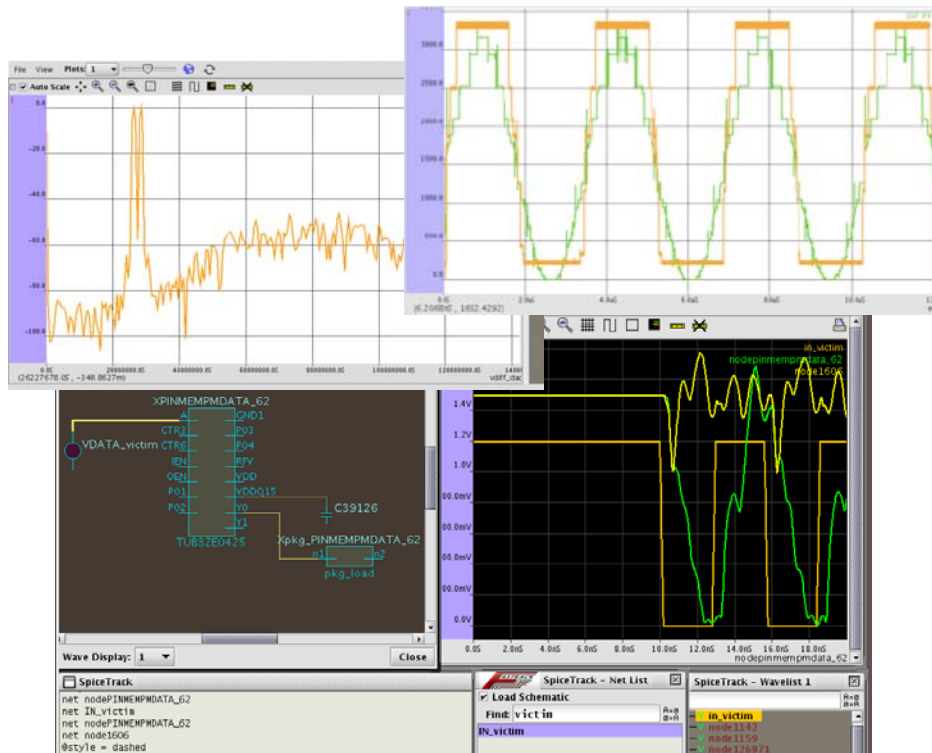


mSPICE

The Only 3G Circuit Simulator

Accuracy is no longer an option - It is a requirement!

mSPICE is a super-high capacity SPICE simulation tool capable of producing 100% accurate SPICE simulation results upto 1000x faster than existing tools. Based on revolutionary patent pending numerical techniques developed at Fastrack Design, mSPICE features increased capacity and user friendly GUI for debugging and analyzing circuits. With its expanded feature set, mSPICE is the ideal tool for custom ASIC, analog, and mixed-signal, pre and post-layout simulations. For nano-meter technologies where signal integrity and mixed-mode signal analysis are particularly critical, mSPICE performs full-chip simulation with no compromise in accuracy.



Benefits

- CAPACITY** with ACCURACY mSPICE boasts 100% accurate SPICE simulation while handling 10+ million devices with no model simplification or data reduction
- SPEED** mSPICE's increased speed and capacity come from superior numerical techniques
 - Linear runtime with netlist size
 - 2-10x faster than existing SPICE
 - 10-100x faster for medium to large netlists (200K transistors)
- COMPATIBILITY** mSPICE offers complete compatibility with many of the industry standard SPICE tools.
 - Supports HSPICE and Spectre netlists, options, and commands
 - Supports BSIM3/4, verilog-A models
 - Supports RAW, FSDB, WDF, TR0, and PSF-ASCII formats
- VERSATILITY** by virtue of the powerful SpiceTrack framework mSPICE can be adapted to various design environments
 - Capable of simulation from only a SPEF netlist as input
 - Capable of reading bit vector formats
 - Configurable output styles to suit different tools
 - TCL interface to allow interactive analysis and debugging

Applications

- Analog circuit design and verification**
Achieve silicon-accurate results for analog circuits such as PLL, ADC, DAC, amplifiers, charge-pumps
- Large mixed-signal and digital circuits**
Supports verilog-A, vector input stimulus. Also enables accurate IO-SSO and power & clock network analysis
- Library characterization**
plug-and-play integration with commercial cell library characterization tools, as well as in-house characterization tools
- Memory verification and characterization**
Enables silicon accurate memory simulation and characterization. A must have for 40nm memory characterization

Results

Design	Size (tr, R, C)	Sim Length	mSPICE runtime	Speed up	mSPICE multi-CPU runtime (4-CPU)
SPLL	4922	30us	18 hours	6X	11 hours
ADC (post-layout)	1.672M	300ns	2.5 hours	∞	1.5 hours
DAC (post-layout)	12904	425us	7 hours	8X	4.75 hours
Decoder	2.5M	500ns	14.5 hours	∞	9 hours
IO-SSO	1.16M	9.9ns	5 hours	∞	1.75 hours
SRAM	64966	34ns	35 mins	∞	12 mins

Technology Features

- Unmatched capacity enables large circuit, post-layout circuit simulation with guaranteed accuracy
- Built-in parallel technology enables further throughput increase without compromising accuracy
- Integrated Java-based GUI enables debugging, analyzing, and viewing results within the same environment