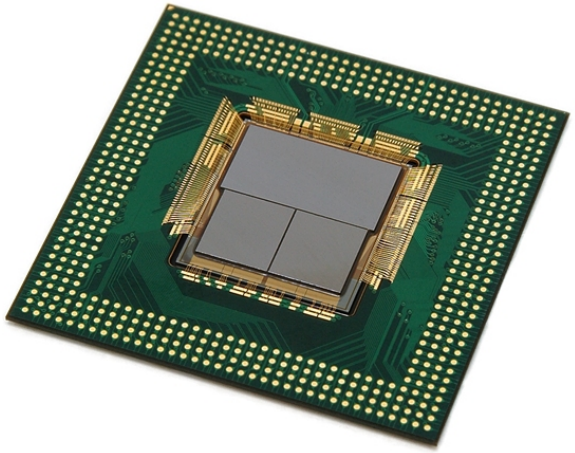
3D IC Multi-chip Architecture

“System-in-Silicon®” Technology

Overview

- System in Silicon(SIS) is developed by SFT(2003-2008) to have spent US $19 millions(15 millions VC and 4 millions NEDO (government) grants.
- SIS was the first introduced in ISSC 2006 and commercially released sample chip in 2007.
- SFT closed business in May 2008.
- 15 patents (including 9 under examination) of SIS's 3D IC technologies moved to new venture company, Liquid Design Systems which was founded by former SFT employees.



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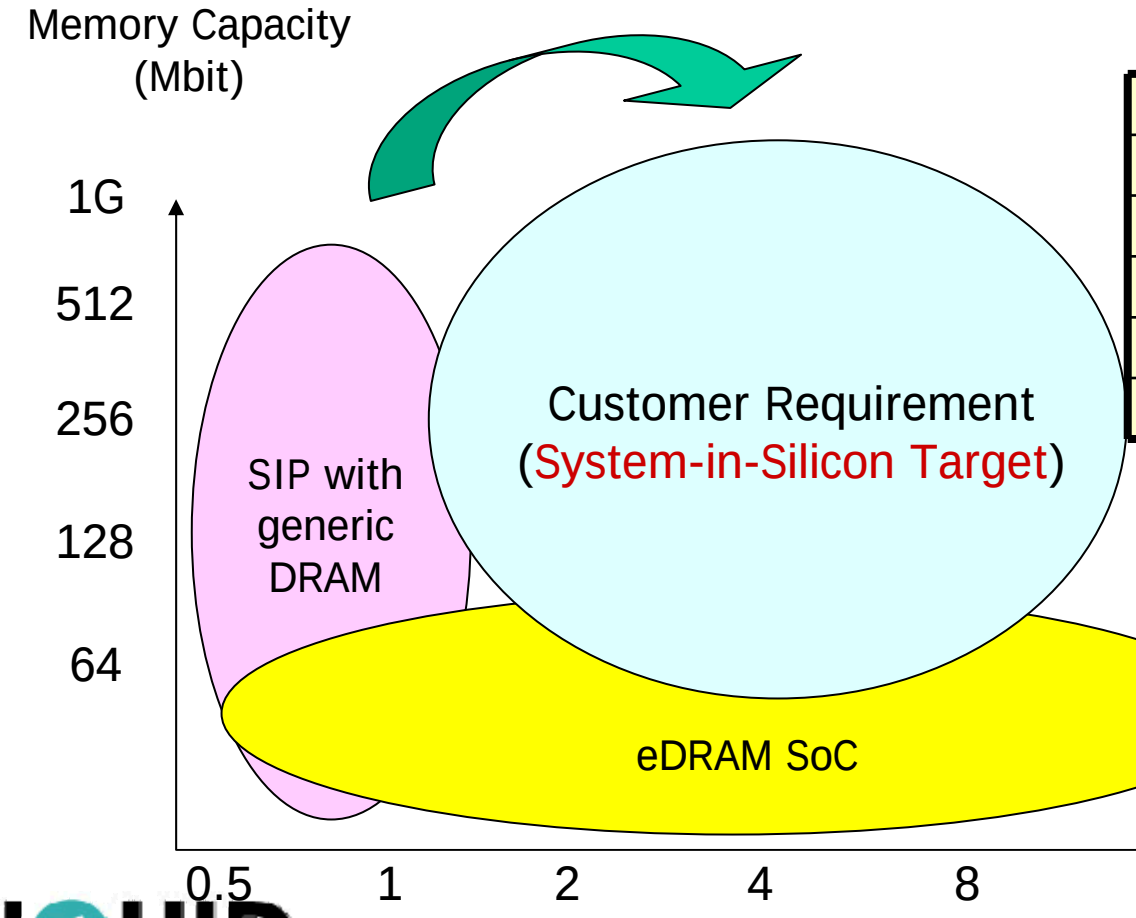
SIS Application target

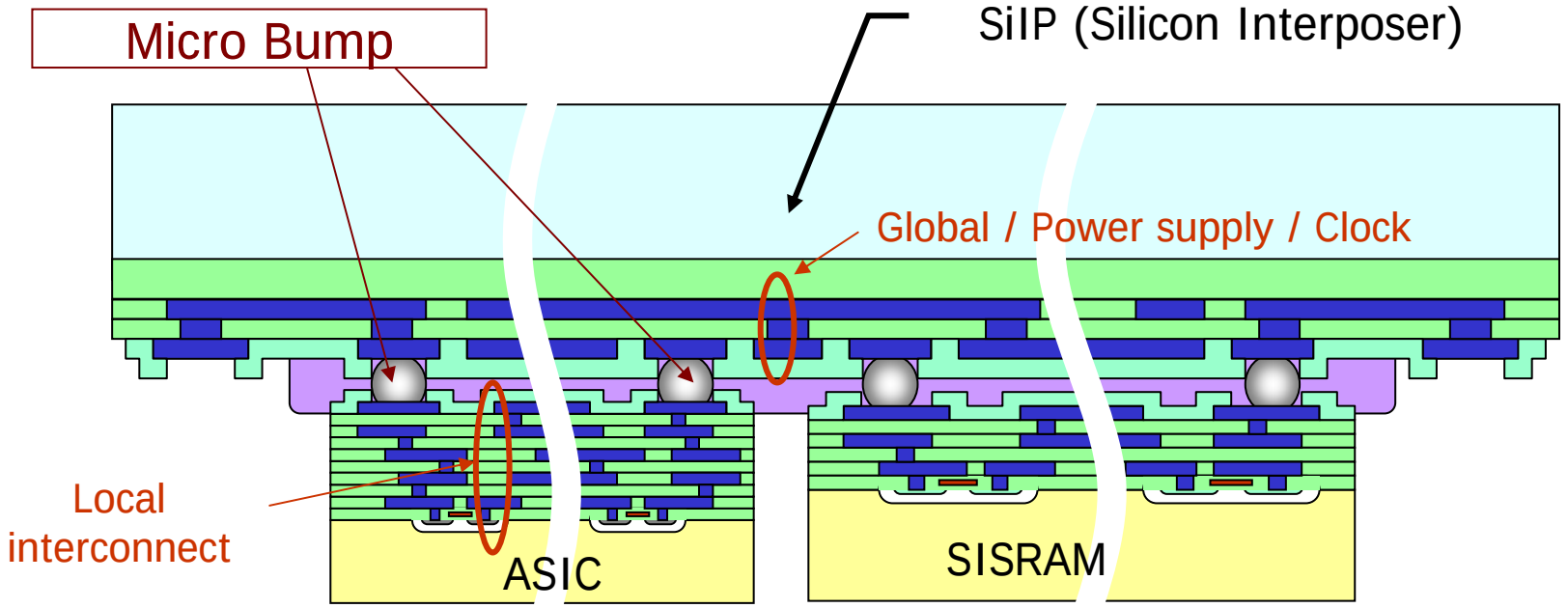
System in Silicon(SIS) is new chip architecture to solve the memory integration with high capacity AND high bandwidth AND low power consumption.



	SIP with generic DRAM	eDRAM SoC
Bus width	NG (~32bit)	OK
Capacity	OK(16M~1G)	NG(~64M)
Power	NG	OK
TTM / TTV	OK	NG
Cost (NRE)	OK	NG
ASIC pin-count	NG (Bonding limit)	OK

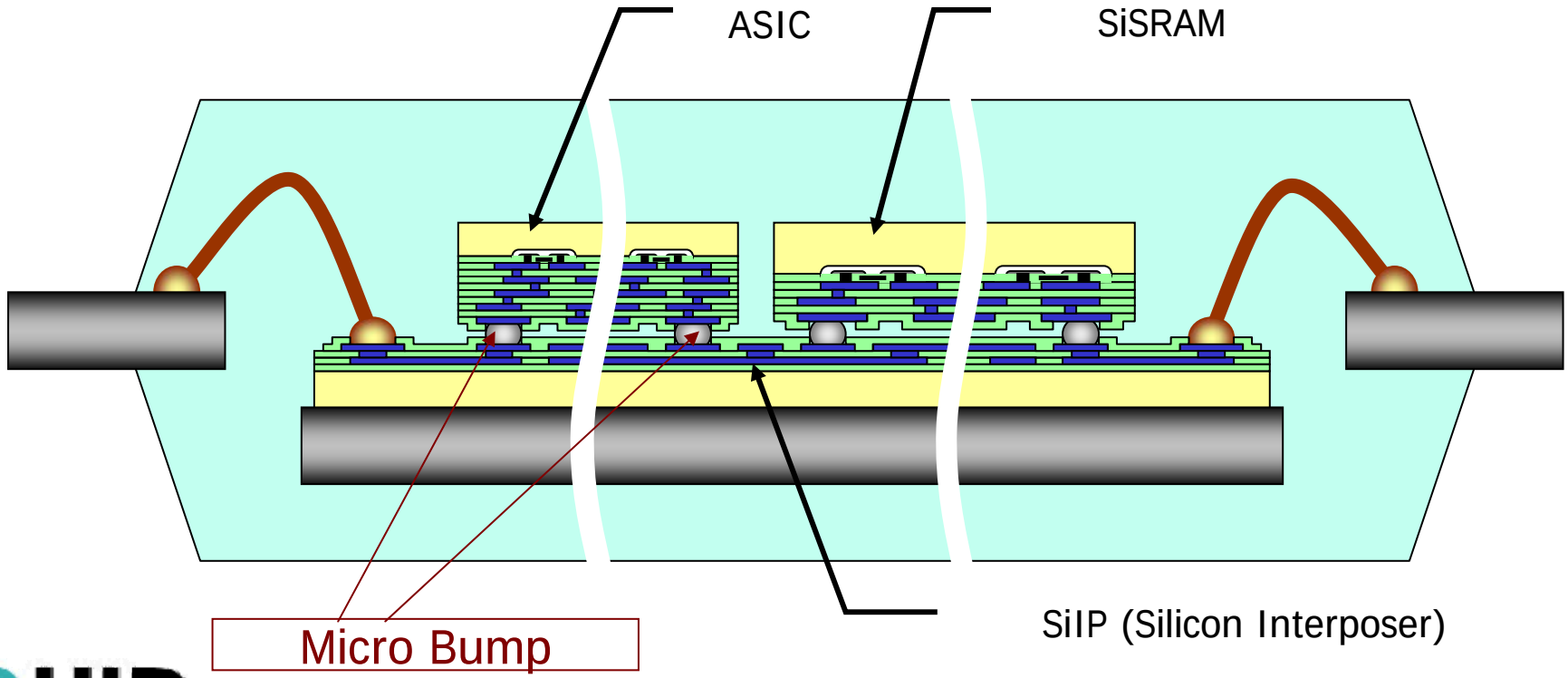
Concept of System-in-Silicon™ Architecture

- SIS is the bridge technology between SoC and PCB
- Silicon interposer will be new solution of the next Chip Jisso
- Micro-bumps for the high density connection



Conventional packaging with SiS Architecture

- Using & improving existing EDA and manufacture equipment
- 10% Lower thermal resistance compared to conventional SoC
- Integration ASIC (logic/SRAM) with RAM, Flash and Analog...



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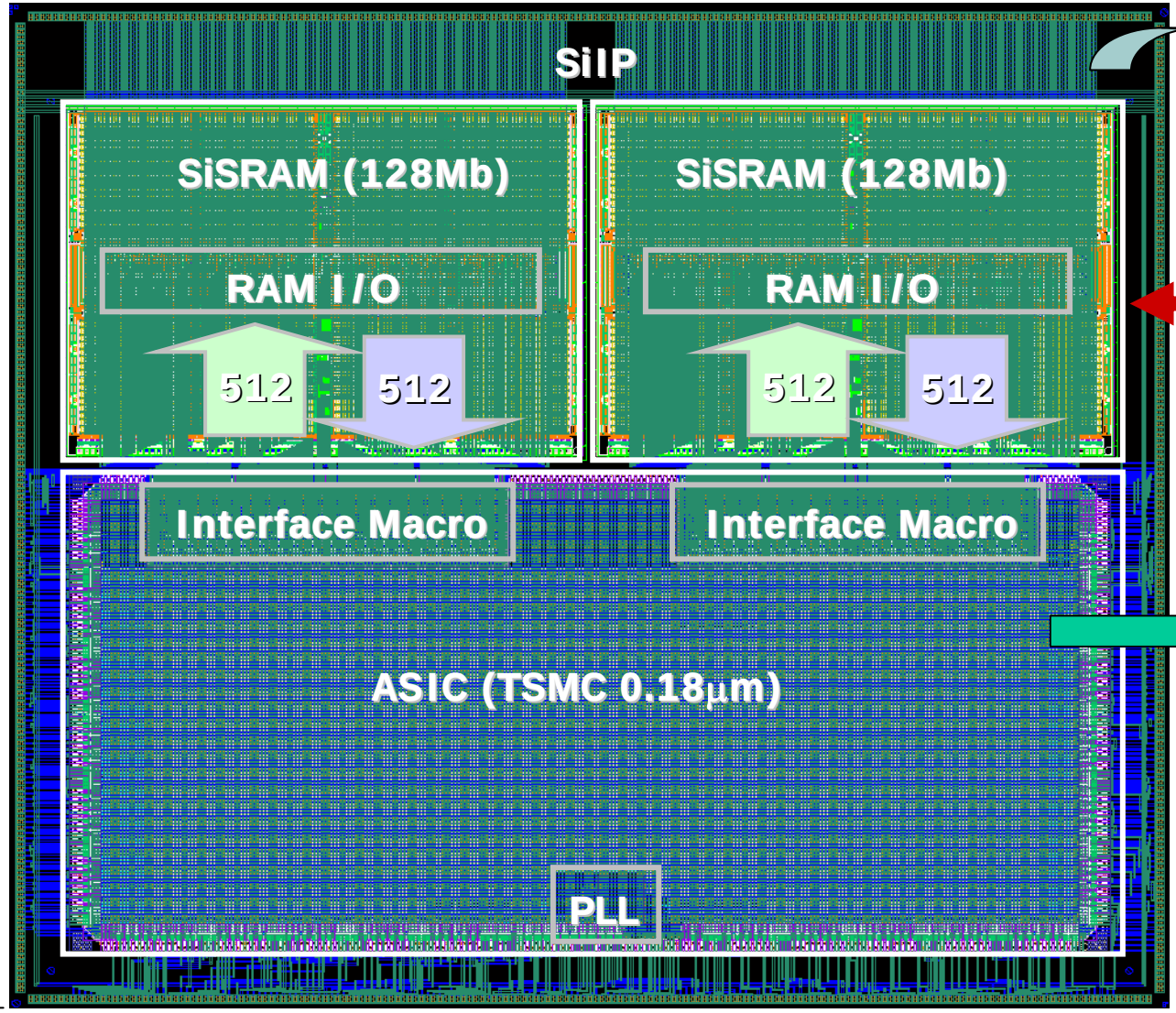
Design of System-in-Silicon®

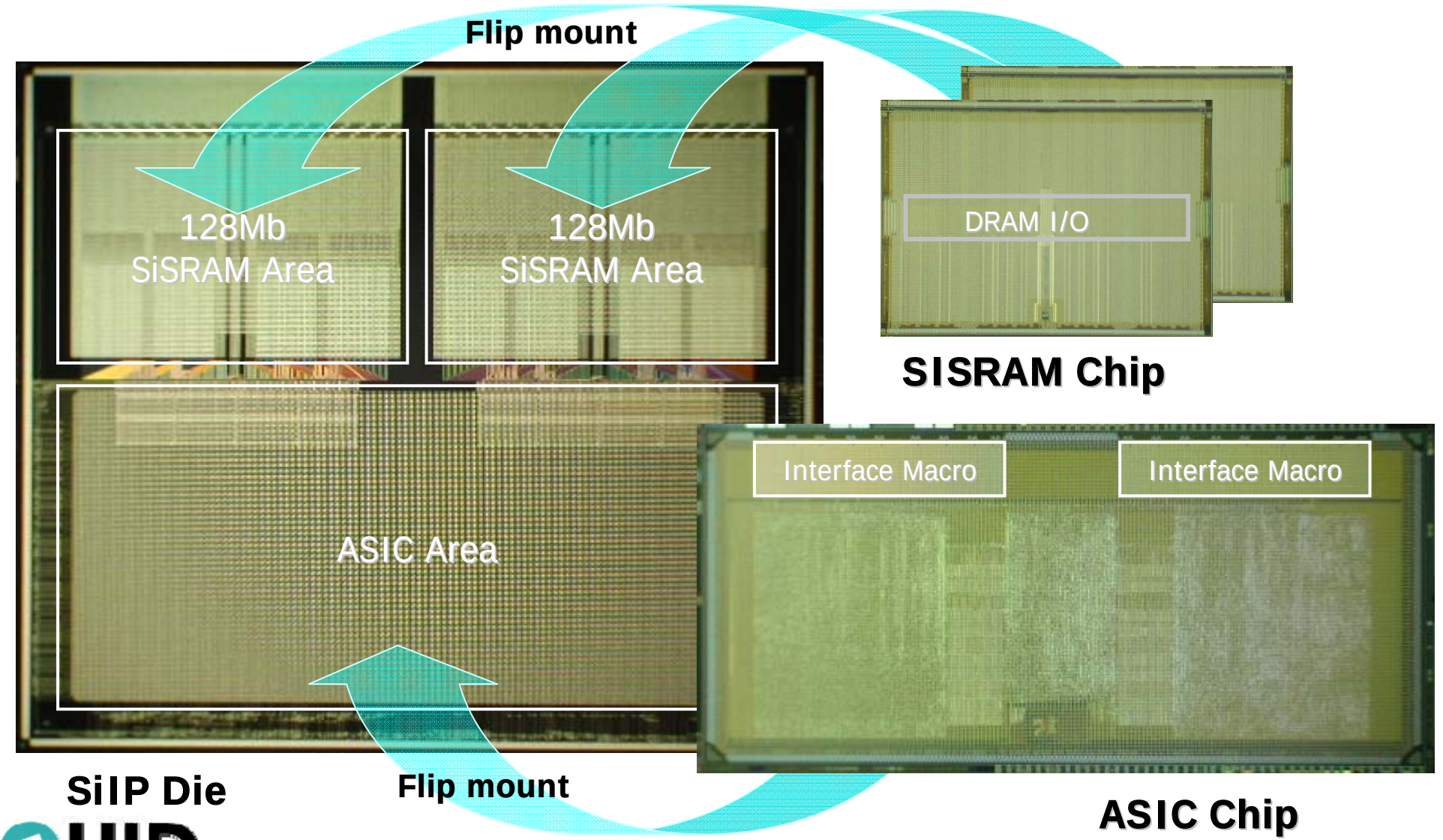


SiIP is taped-out by flipped data

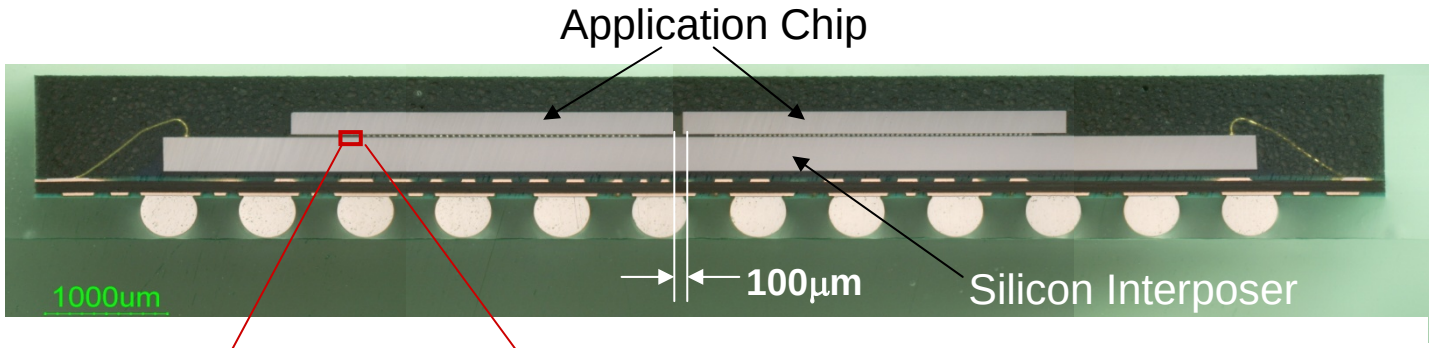
RAM is physical instance (pre-designed)

ASIC is taped-out separately

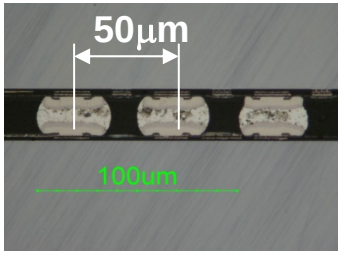
Fabrication of System-in-Silicon®



Chip Example

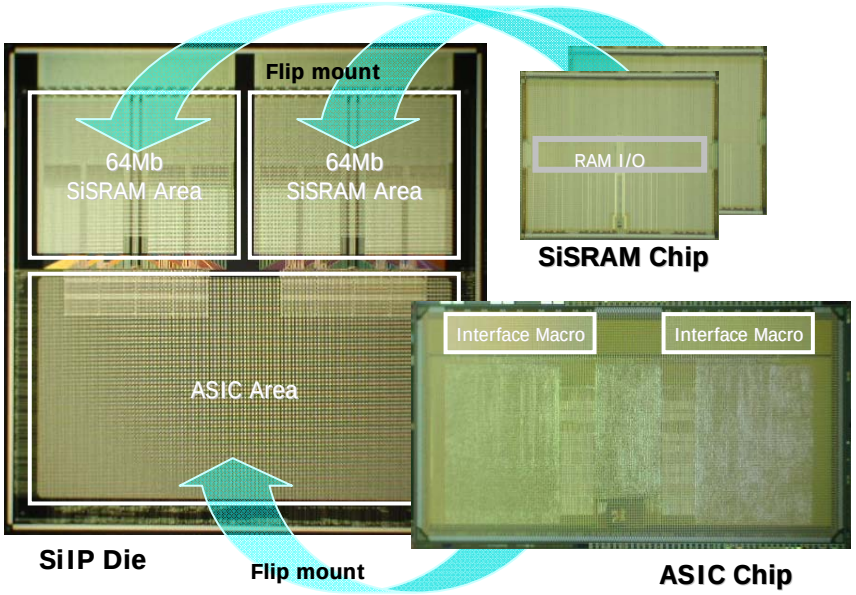


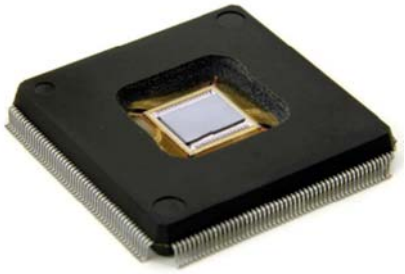
Side-by-Side
144pin-BGA



50μm-pitch
bump

Side-by-Side 256pin-BGA (ISSCC 2006)





Chip-on-Chip
208pin-QFP

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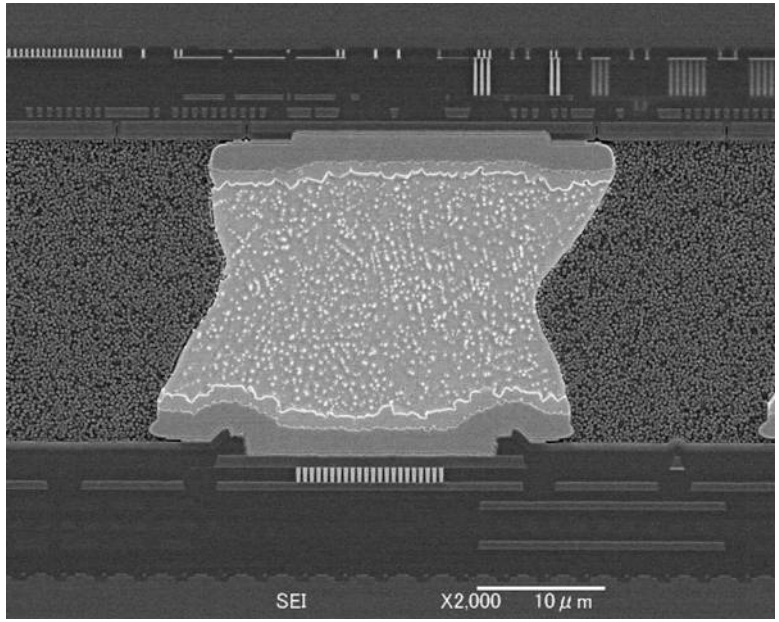
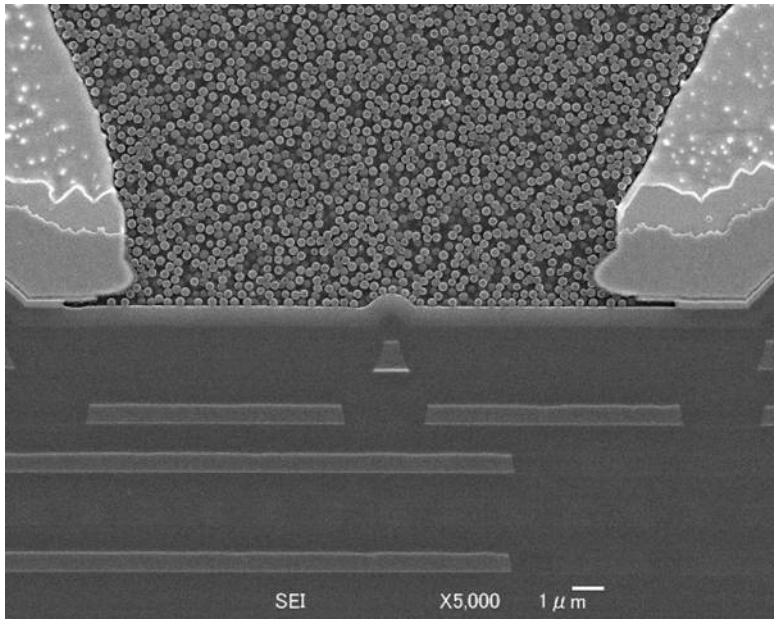
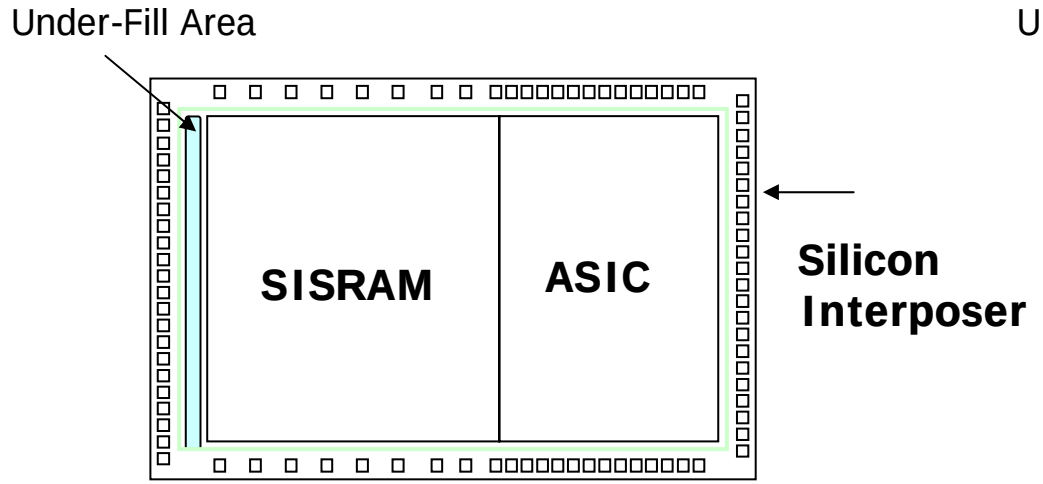
Micro Bump & Under Fill

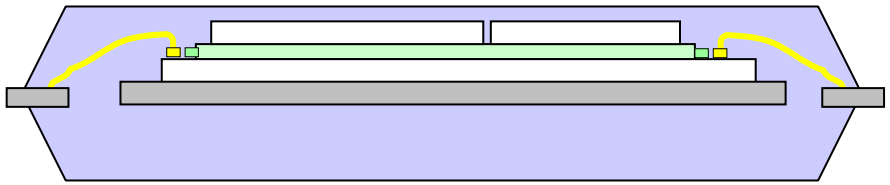




System-in-Silicon: SbS vs CoC

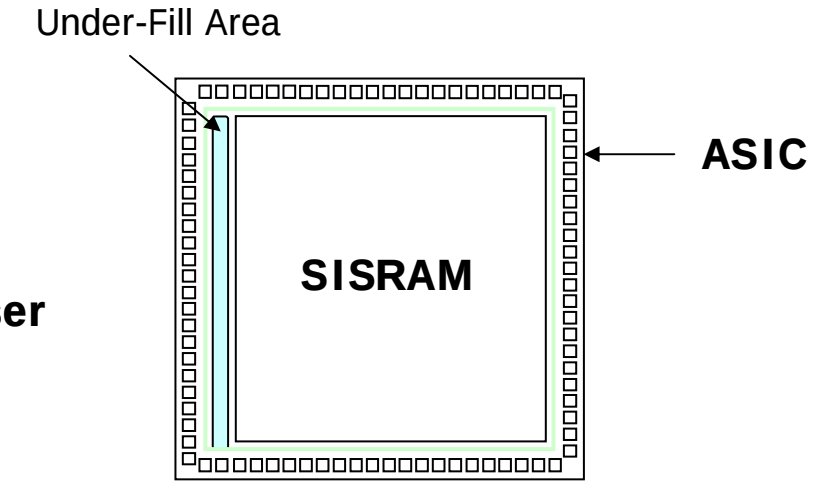
Side-by-Side structure (SbS)

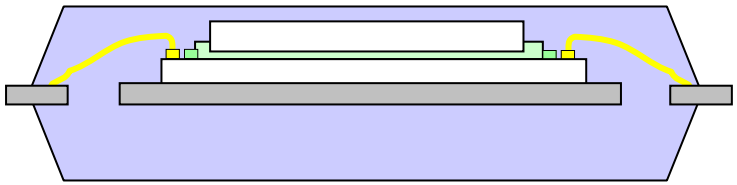




TSV Structure
for mobile application

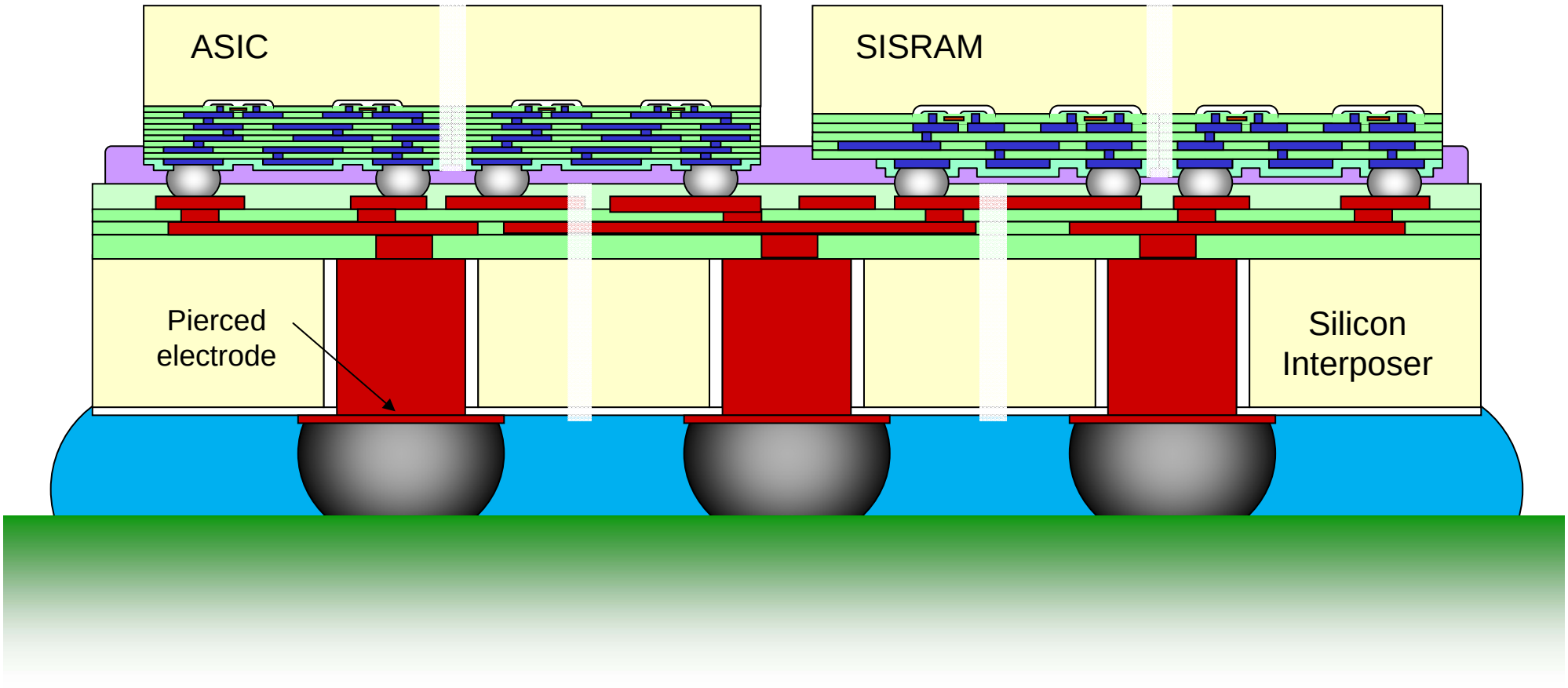
Chip-on-Chip structure (CoC)



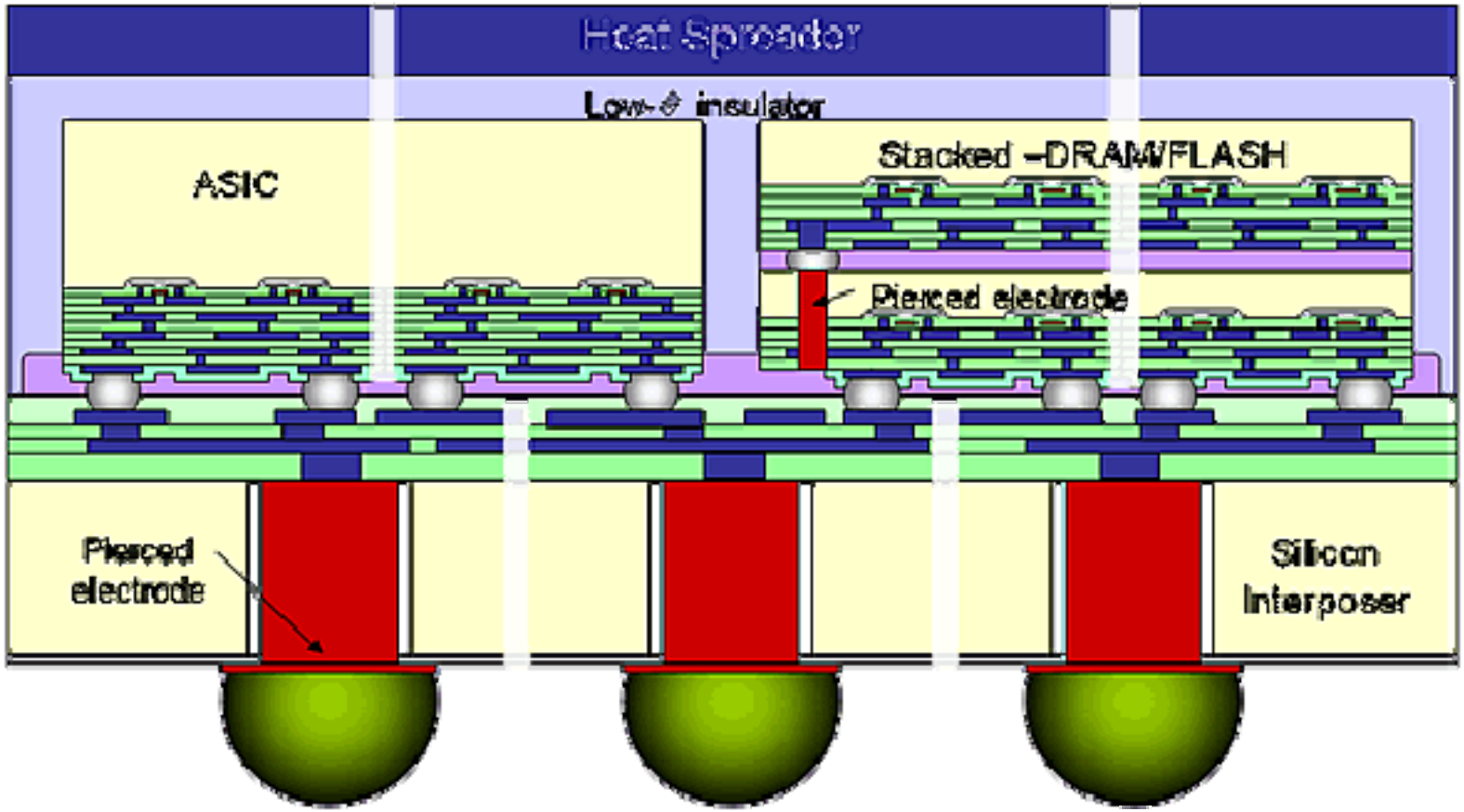


ASIC > SISRAM

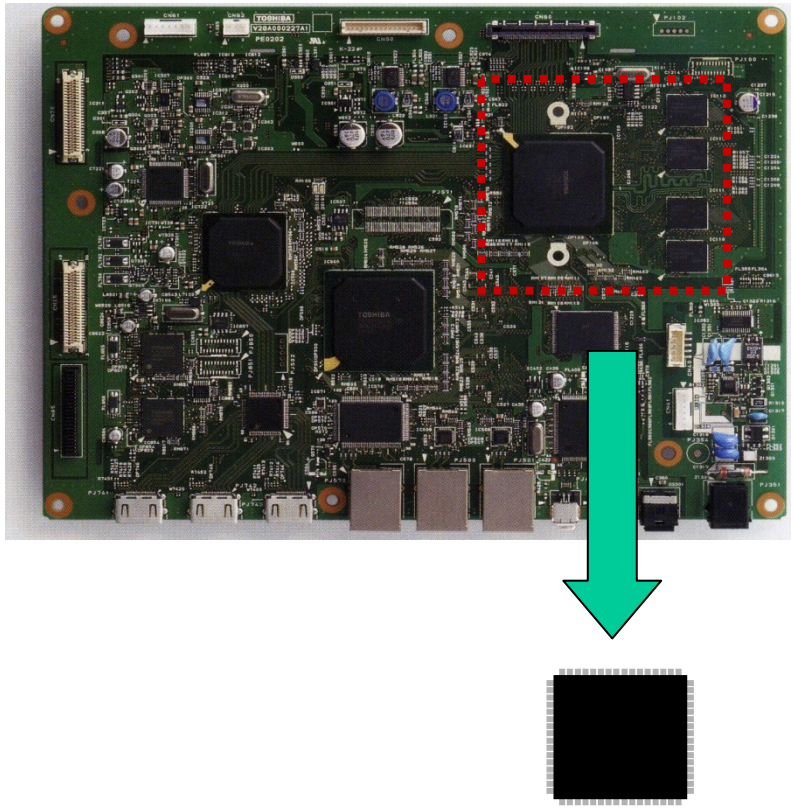
Side-by-side SiS with TSV

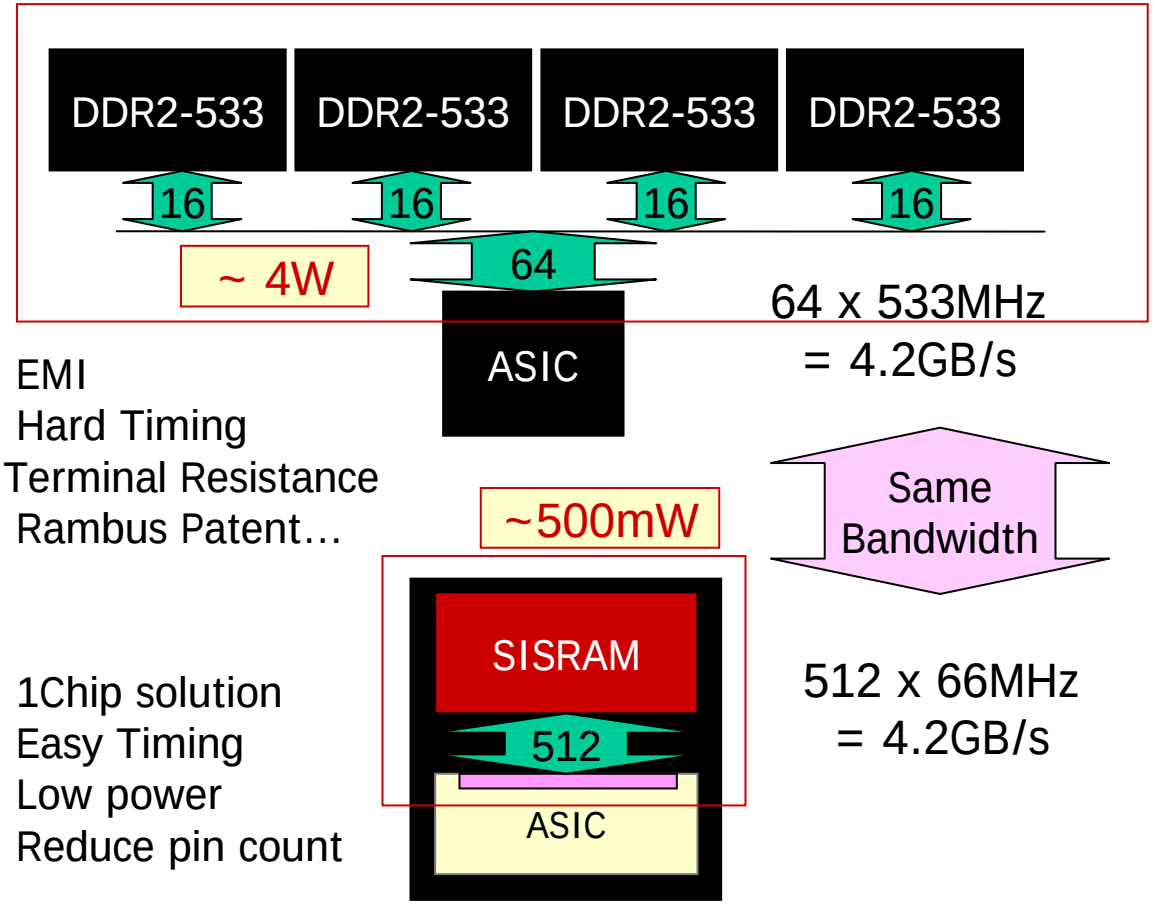


SiS with FLASH (SISFLASH)



System Integration For TV set





- EMI
- Hard Timing
- Terminal Resistance
- Rambus Patent…

- 1Chip solution
- Easy Timing
- Low power
- Reduce pin count

"System-in-Silicon"

Power consumption < 1/8

SISRAM Power consumption

Memory Type	Data Rate	Power for VDD	Power for Interface	Total Power consumption
MobileDDR333 (x32:167MHz) 2 pieces	333Mx32x2/8 =**2.67GB/s**	P=150mAx2x 1.8V=540mW @VDD=1.8V	P=20pFx64x1.2Vx1.2V/ 6ns/2=153.6mW @VDDQ=1.2V CL(I/O)=20pF	Ptotal=540+153.6 = **693.6mW**
256M SISRAM (x256:100MHz) 1 piece	100Mx256/8 =**3.2GB/s**	P=100mAx1.2 V=120mW @VDD=1.2V	P=1.5pFx256x1.2Vx1.2 V/20ns/2=13.9mW @VDDQ=1.2V CL(D/Q)=1.5pF	Ptotal=120+13.9 = **133.9mW**
512M SISRAM (x512:100MHz) 1 piece	100Mx512/8 =**6.4GB/s**	P=100mAx1.2 Vx2=240mW @VDD=1.2V	P=1.5pFx512x1.2Vx1.2 V/20ns/2=27.7mW @VDDQ=1.2V CL(D/Q)=1.5pF	Ptotal=240+27.7 = **267.7mW**

Contact us

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