3D IC Multi-chip Architecture

2010 version
Outline

- Who is Liquid Design Systems?
- Products and Services
- 3D IC Market
- 3D IC Advantage
- SIS architecture demonstration (ISSCC2006)
- Silicon Interposer PKG (ECTC2008)
- Patents
Who is Liquid Design?
LDS Company Overview

Liquid Design Systems, Inc.
Founded June 6, 2008, operation started in Sept.
Officers Naoya Tohyama (CEO)
Takuya Inoue (COO)
Koichi Kumagai (CTO)
Maki Iwasaki (US rep)
KSP 421B 3-2-1 Kawasaki-city,
Kanagawa, Japan 213-0012
Phone: +81-44-814-5544
Facsimile: +81-44-712-8555
http://www.liquiddesign.co.jp
Board members 1/2

Naoya Tohyama  CEO
- CEO, Liquid Design Systems, Inc.
- Before founding Liquid Design Systems in Jun 2008, he served as VP marketing at System Fabrication Technologies, Inc (SFT) as one of 5 founders since 2003.
- Prior to joining SFT, he spent 13 years at Cadence Design Systems, Japan, as marketing director.
- He graduated from State University of New York, Buffalo in 1985, and learned MBA essence course at SANNO Institute of Management in 2008.

Takuya Inoue  COO
- Regional Director of Altium Japan KK. a leading supplier with low price PCB and FPGA CAD, from 2006 to 2008
- Semiconductor Industrial Research Manager at IDC Japan, a global market research firm, from 2003 to 2005
- Operation Manager for PCB & System Business of Cadence Design Systems Japan KK
- Account Manager at Synopsys Japan KK as a lead for Toshiba business
- Sales Representative at Texas Instruments Japan for 9 years after graduating university
- BS of Industrial Engineering at Musashi Institute of Technology
Board members 2/2

Koichi Kumagai, CTO
- 1986-2004 NEC and NEC Electronics ASIC/SoC- circuit design, process design and development
- 2004.8-2008 System Fabrication Technologies, Director of R &D- System in Silicon
- 2009.1 Liquid Design Systems, CTO

Tokinori Kozawa, executive director
- 2008.9 Liquid Design Systems Executive director
- 2006-2008 ASIP Solutions, Inc., Board director
- 1996-2005 Semiconductor Technology Academic Research Center (STARC) Board director
- 1965-2000 Hitachi Central Research Laboratory Chief Engineer, director Membership
  - Fellow, The Institute of Electronics, Information and Communication Engineers, Japan
  - IEEE Computer Society Golden Core Member
  - Design Automation Conference (DAC) Asia committee member (1988-1992)
  - Asia South Pacific Design Automation Conference (ASPDAC) General Chair (1998)
  - Design Automation and Test in Europe committee member as Asian Representative (1998-2002)
  - Euro-DAC Topics Chair (1994-1996)

Shigehisa Wakamatsu, executive director
  - Manager of ASIC (Gate Array, SoC) development group.
  - After the previous group, director of Semiconductors’ IPs (patents) group
- 2004-2008 System Fabrication Technologies, Inc Board director
- 2008.9 Liquid Design Systems, Executive director
SIS® technology was accepted by ISSCC2006 and ECTC2008, presented by Kumagai (CTO)

System-in-Silicon Architecture and its Application to H.264/AVC Motion Estimation for 1080HDTV

IEEE International Solid-State Circuits Conference

IEEE

International Solid-State Circuits Conference
RECOGNIZES

OF System Fabrication Technologies, Yokohama, Japan
Waseda University, Kita-Kyushu, Japan
FOR PRESENTATION OF THE PAPER
System-in-Silicon Architecture and its Application to H.264/AVC Motion Estimation for 1080HDTV
SAN FRANCISCO, CALIFORNIA
FEBRUARY 2006

Nikkei article
Products and Services

- 3D IC Design and Prototyping Service
- Design Service
- 3D IC simulator (under developing)
- ASIC Product Prototyping
3D IC development issues

- System design
- IP Vendor [Memory, IF, Analog...]
- Chip design
- Wafer Fab.
- Assembly
- Test
- Product Out

IP (macro): Plan • Dev. • Design

Waf. Shuttle
- 4~5mm sq./area
- ¥12M@90nm
- 1-2 /month

Eval.
- OK
- Fail

Si proven IP release

3DIC dev. env. issues:
- High cost: Full mask Fab.
- Few Players: IP, EDA Vendor, ...

Solution:
Low cost 3DIC dev. env. w/ Waf. Shuttle
Low Cost 3DIC Prototyping Service

- Prototyping Cost down to 1/5 - 1/10

[ Conventional ]
- Wafer Fab.
- TSV, μBump (Wafer)
- Dicing
- Packaging

[ LSI Shuttle service ]
- Wafer Shuttle
- Dicing
- TSV, μBump (Chip)
- Packaging

LDS Prototyping Service
3D IC Shuttle service concept

Customer
- Shuttle coordinator
- Bare chip
- LDS
- Design Flow, PDK
- Bumping tech.
- Flip Chip Bonding tech.
- Evaluation
- TSV

Module
- Chip with Bump

LDS

Market/Needs

Tech./Seeds
3D IC Design Service

- 3DIC interface design using μ-Bump, TSV, Si-interposer, …
  - Passive element (LCR) development
  - Interface Macro development
- ESD, Driverability optimization

- E.g.): μ-Bump + TSV → Optimization of Chip to Chip interconnect
**3D IC Spice Simulator Concept (under develop)**

<table>
<thead>
<tr>
<th>I/O pin property</th>
<th>Chip property</th>
<th>PCB property</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value of signal</td>
<td>Netlist</td>
<td>RCGL extraction</td>
</tr>
<tr>
<td># of pins</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock timing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Waveform generation</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3DIC Verification System
- Simulation engine core is provided by mSPICE
- Simulation pre-processing flow control is based on Tcl
- User interface to check the QoR
- Product code will be “SPICE TRACK – 3DIC

Waveform Value table

Analysis on Waveform Viewer
QoR Check
3D IC market
Chips/3D IC Market to Reach US$5.2 Billion by 2015


- GIA announces the release of a comprehensive global market report on 3D Chips (3D IC) market. The global market for 3D Chips is forecast to reach US$5.2 billion by the year 2015. Key factors driving market growth include exceptional features and benefits offered by the chips, and increasing demand from existing and niche market applications. Further, the shift towards miniaturization, digitalization and high-speeds continue to shape fortunes of 3D Chips.
System in Silicon (SIS) is a new chip architecture to solve the memory integration with high capacity AND high bandwidth AND low power consumption.

Customer Requirement *(System-in-Silicon Target)*

- **Memory Capacity** (Mbit)
  - 1G
  - 512
  - 256
  - 128
  - 64

- **Bandwidth (GB/s)**
  - 0.5
  - 1
  - 2
  - 4
  - 8
  - 16

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SIP with generic DRAM</th>
<th>eDRAM SoC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus width</td>
<td>NG (~32bit)</td>
<td>OK</td>
</tr>
<tr>
<td>Capacity</td>
<td>OK (64M~1G)</td>
<td>NG (~64M)</td>
</tr>
<tr>
<td>Power</td>
<td>NG</td>
<td>OK</td>
</tr>
<tr>
<td>TTM / TTV</td>
<td>OK</td>
<td>NG</td>
</tr>
<tr>
<td>Cost (NRE)</td>
<td>OK</td>
<td>NG</td>
</tr>
<tr>
<td>ASIC pin-count</td>
<td>NG (Bonding limit)</td>
<td>OK</td>
</tr>
</tbody>
</table>
The integration of 3D technologies will enable performances, form factor and cost requirements of the next generation of electronic devices:

- "More than Moore" Heterogeneous integration
  - Co-integration of RF + logic + memory + sensors in a reduced space

- Electrical performances
  - Interconnect speed and reduced parasitances

- Density
  - Achieving the highest capacity / volume ratio

3D vs. "More Moore"
- Can 3D be cheaper than going to the next lithography node?

Source: Yole development 2008
3D Silicon/glass interposer wafer forecast by application

Source: Yole development 2010
SIS 3DIC target and Market

Target for 3D Graphics for mobile phone
Hi-end PC, EWS

DDR3
512M
256M
128M
64M
1G

Capacity

DDR2

65nm eDRAM
90nm eDRAM

TV application

256M-SISRAM
25mm2 / x256 @ 133MHz

512M-SISRAM
50mm2 / x512 @ 133MHz

128M-SISRAM x2
90mm2

64M-SISRAM x2
70mm2

128M-SISRAM
45mm2

64M-SISRAM
35mm2

64M

512M

256M

128M

64M

1G

Capacity

Bandwidth
[GB/sec]
3D IC advantage
Benefit of SiS (SiIP + side by Side) structure

- ~ Fan ~ 4W
- ~ no FAN ~ 1W
- ~ 4W

- EMI
- Hard Timing
- Terminal Resistance
- Rambus Patent...

- 1Chip solution
- Easy Timing
- Low power
- Reduce pin count

- 64 x 533MHz = 4.2GB/s
- 1024 x 66MHz = 8.4GB/s

“System-in-Silicon”

Power < 1/4

~ 1W

DDR2-533 DDR2-533 DDR2-533 DDR2-533
16 16 16 16

64 x 533MHz = 4.2GB/s

Bandwidth

~ 1W

~ 4W
## Power consumption compared with DDR

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Data Rate</th>
<th>Power for VDD</th>
<th>Power for Interface</th>
<th>Total Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>MobileDDR333 (x32:167MHz)</td>
<td>333Mx32x2/8</td>
<td>P=150mA x2x1.8V=540mW @VDD=1.8V</td>
<td>P=20pFx64x1.2Vx1.2V/6ns/2=153.6mW @VDDQ=1.2V CL(I/O)=20pF</td>
<td>Ptotal=540+153.6 = 693.6mW</td>
</tr>
<tr>
<td>256M SISRAM (x256:100MHz)</td>
<td>100Mx256/8</td>
<td>P=100mA x1.2V=120mW @VDD=1.2V</td>
<td>P=1.5pFx256x1.2Vx1.2V/20ns/2=13.9mW @VDDQ=1.2V CL(D/Q)=1.5pF</td>
<td>Ptotal=120+13.9 = 133.9mW</td>
</tr>
<tr>
<td>512M SISRAM (x512:100MHz)</td>
<td>100Mx512/8</td>
<td>P=100mA x1.2Vx2=240mW @VDD=1.2V</td>
<td>P=1.5pFx512x1.2Vx1.2V/20ns/2=27.7mW @VDDQ=1.2V CL(D/Q)=1.5pF</td>
<td>Ptotal=240+27.7 = 267.7mW</td>
</tr>
</tbody>
</table>
Using Silicon interposer V.S. CoC

SiS with silicon interposer

Chip-on-Chip structure (CoC) with out silicon interposer

Under-Fill Area

TSV Structure for mobile application

ASIC > SI SRAM

Silicon Interposer
SiS with TSV architecture

SIQRAM

Pierced electrode

Silicon Interposer
SIS architecture demonstration (ISSCC 2006)

“System-in-Silicon Architecture and its Application to H.264/AVC Motion Estimation for 1080HDTV”
System-in-Silicon® Architecture

- SIS is the bridge technology between SoC and PCB
- Block-base SoC design and multi-chip fabrication
- System is encapsulated by Silicon (→ SiS)
- Global routing over different substrates using SiIP
- Micro-bumps for the high density connection

Micro Bump

SiIP (Silicon Interposer)

Global / Power supply / Clock

Local interconnect

ASIC

SiS-RAM
Packaging with SIS® Architecture

- Using & improving existing EDA and manufacture equipment
- 10% Lower thermal resistance compared to conventional SoC
- Integration ASIC (logic/SRAM) with RAM, Flash and Analog…

ASIC

Memory(SISRAM)

Micro Bump

SiIP (Silicon Interposer)
Design of System-in-Silicon®

SiIP is taped-out by flipped data.

ASIC is taped-out separately.

RAM is a physical instance (pre-designed).

SiIP is taped-out by flipped data.

ASIC is taped-out separately.
Silicon interposer PKG
(ECTC 2008)
“A Silicon Interposer BGA Package with Cu-Filled TSV and Muti-Layer Cu-Plating Interconnect”
Silicon Interposer PKG Structure

- **Si substrate**
- **Cu-filled TSV** (~60\(\mu\)m\(\phi\))
- **t = 200~300\(\mu\)m**
- **SnAg BGA Outer Ball**
- **Micro-bumps (40~50\(\mu\)m pitch)**
- **SMT applicable Ball pitch (e.g. 800\(\mu\)m)**
- **Memory / Application Chip (FC mounted)**
- **Fine pitch Multi-Layer Cu-RDL**
- **Insulation layer (T-SiO2)**
- **Under-fill Resin**

**PKG Structure**
Key Technologies for Silicon interposer PKG

1. Cu-filled TSV
2. Multi-layer Cu-RDL
3. Micro-bump interconnect
Silicon interposer PKG Test Chip

(a) Top View

Chip 1
50µm pitch
2,964 µBumps

Chip 2
40µm pitch
4,615 µBumps

Chip 3
50µm pitch
2,024 µBumps

Chip 4
50µm pitch
1,886 µBumps

Sil P with TSVs

(b) Bottom View

0.8mm pitch, 0.45mmϕ

BGA Outer Ball
# Silicon interposer PKG Test Chip Summary

<table>
<thead>
<tr>
<th>SiIP PKG</th>
<th>144pin BGA (12x12 Ball Array)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiIP</td>
<td></td>
</tr>
<tr>
<td>Body size</td>
<td>11 mm x 11 mm</td>
</tr>
<tr>
<td>Thickness</td>
<td>200μm</td>
</tr>
<tr>
<td>TSV</td>
<td></td>
</tr>
<tr>
<td>pitch</td>
<td>800μm</td>
</tr>
<tr>
<td>Diameter</td>
<td>60μm</td>
</tr>
<tr>
<td>Cu</td>
<td></td>
</tr>
<tr>
<td>L/S (Min.)</td>
<td>4μm / 4μm</td>
</tr>
<tr>
<td>Cu Thickness</td>
<td>3μm</td>
</tr>
<tr>
<td>RDL (2L)</td>
<td></td>
</tr>
<tr>
<td>Via Diameter</td>
<td>10μm</td>
</tr>
<tr>
<td>FC Mounted Chips</td>
<td></td>
</tr>
<tr>
<td>Chip size</td>
<td>3.35 mm x 3.1 mm</td>
</tr>
<tr>
<td>Thickness</td>
<td>200 μm</td>
</tr>
<tr>
<td>Micro-bump pitch</td>
<td>50μm (Chip 1,3,4), 40μm (Chip2)</td>
</tr>
</tbody>
</table>
Silicon interposer PKG Cross-section

Inter-chip space: 100\(\mu\)m

Chip 2: 40\(\mu\)m Bump pitch

Chip 1: 50\(\mu\)m Bump pitch

TSV

Outer Ball Land

TSV/Outer Ball pitch: 800\(\mu\)m

Silicon interposer PKG Cross-section - section
Cu Plating
UBM / Bump formation
Memory/Application Chip
Wafer Process (FEOL/BEOL)
Wafer sort
UBM / Bump formation
Wafer thinning (Back side grinding)
Dicing
Silicon interposer PKG Fabrication Flow
SiP
Si Waf.
Wafer thinning (Back side grinding)
Via etching
Insulation
Metal Filling
Multi-layer wiring
UBM / Bump formation
Chip mount on wafer
Outer ball formation
Dicing
Final Test
Silicon interposer Top view before FC Mount

50 μm pitch micro-bump array

TSV LAND: 800 μm pitch
Wiring Length Comparison

-64%
-71%

Print Board
Bonding Wire
SilP

Ref. G6
SiIP PKG.
Al
Cu

Ref. G7
SiIP PKG.
Al
Cu

Outer Ball Position
Silicon interposer PKG Design Flow

- Almost same as the SoC design Flow
  ➔ Short design TAT

- Hierarchical Partitioning

- Sil P PKG Top-level Design
  - Floor Planning
  - Hierarchical Flattening
    - Place & Route
    - RC-Extract
    - STA
    - DRC/LVS
  - LayoutTiming

- ASIC Design
  - Net-list
  - ASIC Mask Data
  - Timing
  - RC-Extract
  - STA
  - DRC/LVS

- Sil P Design
  - Place & Route
  - GDSII
  - Mask Data
  - Timing
  - RC-Extract
  - STA
  - DRC/LVS
  - Layout

- Sil P PKG Top-level Verification
Contact

- Liquid Design Systems, Inc
- Founded June 6 2008
- C.E.O. Naoya Tohyama
- C.O.O. Takuya Inoue
- C.T.O. Koichi Kumagai
- Office KSP 421B Sakado 3-2-1 Takatsu-ku, Kawasaki-shi
- Tel 81-44-814-5544
- Mail lds.tohyama@liquiddesign.co.jp
LDS provides

- We are able to provide 3D IC design and implementation service.
- All our LDS members are speak English, and can provide English based information.
- We have thousands of 3D IC technologies data from real chip design and test, some of them are old for now, but they are still useful to reduce TAT and cost for development.
- We have several 3D IC partners in Japan, and can transfer their specific skill to you.
谢谢
감사합니다
Thank you
ありがとうございます